1. A method to form MOS gates in an integrated circuit device comprising:

forming a dielectric layer overlying a substrate;

forming a polysilicon layer overlying said dielectric layer;

forming a silicon oxide layer overlying said polysilicon layer;

forming a patterned masking layer overlying and selectively exposing said silicon oxide layer;

thereafter oxidizing said polysilicon layer to increase thickness of said exposed silicon oxide layer wherein said thickened silicon oxide layer encroaches under the edges of said masking layer and wherein said silicon oxide layer does not thicken under other interior areas of said masking layer;

thereafter removing said masking layer;

thereafter etching said silicon oxide layer to selectively expose said polysilicon layer where said silicon oxide layer did not thicken; and

thereafter etching through said exposed polysilicon layer to thereby form MOS gates in the manufacture of said integrated circuit device.

2. The method according to Claim 1 wherein said MOS gates

comprise floating gates for split gate flash devices.

3. The method according to Claim 1 wherein said step of forming a silicon oxide layer comprises thermal oxidation of said polysilicon layer.

4. The method according to Claim 1 wherein said step of thereafter etching said silicon oxide layer to selectively expose said polysilicon layer comprises an oxide dip.

5. The method according to Claim 1 wherein said MOS gates have a dish-shaped cross-sectional profile.

6. The method according to Claim 1 wherein said masking layer comprises silicon nitride.

7. The method according to Claim 1 wherein edges of said MOS gates overlie isolation structures in said substrate.

8. A method according to Claim 1 further comprising:

removing said silicon oxide layer after said step of etching through said exposed polysilicon layer;

thereafter etching said MOS gates to selectively expose said substrate;

thereafter forming a second dielectric layer overlying said MOS gates and said exposed substrate;

depositing a second conductor layer overlying said second dielectric layer; and

etching back said second conductor layer to form second MOS gates on sidewalls of said MOS gates.

9. The method according to Claim 8 wherein said second MOS gates comprise control gates for split gate flash devices.

10. A method to form split gate flash devices in an integrated circuit device comprising:

forming a dielectric layer overlying a substrate;

forming a polysilicon layer overlying said dielectric layer;

forming a silicon oxide layer overlying said polysilicon layer;

forming a patterned masking layer overlying and selectively exposing said silicon oxide layer;

thereafter oxidizing said polysilicon layer to increase thickness of said exposed silicon oxide layer wherein said thickened silicon oxide layer encroaches under

the edges of said masking layer and wherein said silicon oxide layer does not thicken under other interior areas of said masking layer;

thereafter removing said masking layer;

thereafter etching said silicon oxide layer to selectively expose said polysilicon layer where said silicon oxide layer did not thicken;

etching through said exposed polysilicon layer to thereby form floating gates;

thereafter removing said silicon oxide layer;

thereafter etching said floating gates to selectively expose said substrate;

thereafter forming a second dielectric layer overlying said floating gates and said exposed substrate;

depositing a conductor layer overlying said second dielectric layer; and

etching back said conductor layer to form control gates on sidewalls of said floating gates in the formation of said split gate flash devices in the manufacture of said integrated circuit device.

11. The method according to Claim 10 wherein said step of forming a silicon oxide layer comprises thermal oxidation of said polysilicon layer.

12. The method according to Claim 10 wherein said second conductor layer comprises polysilicon.

13. The method according to Claim 10 wherein said step of thereafter etching said silicon oxide layer to selectively expose said polysilicon layer comprises an oxide dip.

14. The method according to Claim 10 wherein said floating gates have a dish-shaped cross-sectional profile.

15. The method according to Claim 10 wherein edges of said floating gates overlie isolation structures in said substrate.

16. An integrated circuit device comprising:

a dielectric layer overlying a substrate;

a patterned polysilicon layer overlying said dielectric layer;

a patterned silicon oxide layer overlying said patterned polysilicon layer wherein said patterned silicon oxide layer is substantially thinner at external edges than at internal areas and wherein external edges of said patterned polysilicon layer and said patterned silicon

oxide layer external edges are aligned.

17. The device according to Claim 16 wherein said patterned polysilicon layer comprises a gate for a MOS transistor.

18. The device according to Claim 16 wherein said patterned polysilicon layer comprises a floating gate for a non-volatile memory cell.

19. The device according to Claim 16 wherein said external edges of said patterned polysilicon layer overlie isolation structures in said substrate.

20. The device according to Claim 16 wherein said patterned polysilicon gate has a dish-shaped cross-sectional profile.